When the output of the pulse counting circuit 173 becomes high level, the AND gate 174 passes the output of the voltage comparator 66 to the pulse duration measuring circuit 175 of the next stage. The pulse duration measuring circuit 175 measures the input pulse duration of the output signal from the AND gate 174, and also integrates the result of measurement. The durations of the high voltage pulse generated frequently are accumulated and when the value exceeds the predetermined accumulation period, the output of the pulse duration measuring circuit 175 becomes high level.

When this high level signal is inputted, the timer circuit 181 in the output control section 180 operates. Thereby the signal inputted to the output control circuit 182 becomes high level for the predetermined period (for example, 1 sec). While the timer circuit 181 is in the operative condition, the output control circuit 182 inputs the low level signal to the AND gate 69. Thereby, the control operation is executed so that the power transistor 61 is turned off to stop the power generation.

In this embodiment, power generation is stopped when output from the output control circuit 182 is in the low level. However, it is also possible to realize duty-control for the on/off conditions of the power transistor 61 by presetting output of the output control circuit 182 to alternately repeat the low level and high level conditions in the predetermined duty ratio.

Moreover, control of power generation is also allowed through setting the power transistor 61 to on/off conditions to set a phase voltage of a certain phase of the armature winding

3 lower than the open voltage of the battery 2.

When the timer 181 terminates the operation, the reset pulse is sent to the pulse duration measuring circuit 175 and pulse counting circuit 173. Thereby the data of the accumulated period and the pulse counting value are reset.

Fig. 12 shows the pulse counting circuit 173. As shown in Fig. 12, the pulse counting circuit 173 is structured with a JK flip-flop circuits 190, 191, a RS flip-flop circuit 192, and inverters 193, 194, 195.

Fig. 13 is a timing diagram illustrating the signal waveforms inputted or outputted to or from each section of the pulse counting circuit 173.

Under the condition that the high level signal is inputted to the reset terminals R of the JK flip-flop circuits 190, 191 and RS flip-flop circuit 192. These flip-flop circuits are reset, and the output Q0 of the JK flip-flop circuit 190 and the output Q1 of the JK flip-flop circuit 191 become low level. Thereby, the output of the inverter 193 becomes high level and this high level signal is applied to the input terminal J of the JK flip-flop circuit 190 of the first stage, while the low level signal is applied to the input terminal K, respectively. Thereafter, when the reset condition is cancelled, the output Q0 of the JK flip-flop circuit 190 becomes high level in synchronization with the rising edge of the pulse signal to be inputted to the clock terminal CK.

In this case, the output Q1 of the JK flip-flop circuit 191 of the second stage is in the low level. Moreover, the output

of the inverter 193 changes to the low level, because the output Q0 of the JK flip-flop circuit 191 has become high level. Accordingly, the low level signal is inputted to the input terminal J of the JK flip-flop circuit 190 of the first stage, and the high level signal to the input terminal K, respectively.

The output Q1 of the JK flip-flop circuit 191 of the second stage becomes high level in synchronization with the rising edge of the next pulse signal, and thereby the output Q0 of the JK flip-flop circuit 190 of the first stage becomes low level.

When the output Q1 of the high level of the JK flip-flop circuit 191 is inputted to the input terminal S of the RS flip-flop circuit 192, the output Q of the RS flip-flop circuit 192 becomes high level. This high level condition is maintained until the reset pulse is inputted to the reset terminal R.

As explained above, the first input pulse signal of the pulse counting circuit 173 is made invalid and the second and subsequent pulse signals are made valid to change the output to the high level.

The voltage regulator 6 of this embodiment detects conditions of a high voltage pulse appearing at the output terminal of the alternator 1 connected to the power supply line 8, and discriminates the condition of a single high voltage pulse generated particularly when a failure is not a connection failure of the power supply line 8 and an electric load of comparatively large capacitance is no longer used and the condition of a high voltage pulse that is irregularly and repeatedly generated in the short period when a connection failure occurs because the